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\* Design Summary \*

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Top Level Output File Name : MIPS\_top\_module.ngc

Primitive and Black Box Usage:

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# BELS : 221

# GND : 1

# INV : 1

# LUT1 : 4

# LUT3 : 2

# LUT4 : 6

# LUT5 : 32

# LUT6 : 91

# MUXCY : 46

# VCC : 1

# XORCY : 37

# FlipFlops/Latches : 53

# FD : 51

# LD : 2

# RAMS : 14

# RAM32M : 10

# RAM32X1D : 4

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 129

# OBUF : 129

Device utilization summary:

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Selected Device : 6slx9tqg144-3

Slice Logic Utilization:

Number of Slice Registers: 53 out of 11440 0%

Number of Slice LUTs: 184 out of 5720 3%

Number used as Logic: 136 out of 5720 2%

Number used as Memory: 48 out of 1440 3%

Number used as RAM: 48

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 193

Number with an unused Flip Flop: 140 out of 193 72%

Number with an unused LUT: 9 out of 193 4%

Number of fully used LUT-FF pairs: 44 out of 193 22%

Number of unique control sets: 2

IO Utilization:

Number of IOs: 130

Number of bonded IOBs: 130 out of 102 127% (\*)

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

WARNING:Xst:1336 - (\*) More than 100% of Device resources are used

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

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clk | BUFGP | 65 |

N0 | NONE(control/ALUsrc) | 2 |

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INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer\_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: 5.121ns (Maximum Frequency: 195.265MHz)

Minimum input arrival time before clock: No path found

Maximum output required time after clock: 6.875ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'

Clock period: 5.121ns (frequency: 195.265MHz)

Total number of paths / destination ports: 10373 / 149

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Delay: 5.121ns (Levels of Logic = 5)

Source: pc/out\_3\_1 (FF)

Destination: alu/zero (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: pc/out\_3\_1 to alu/zero

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 2 0.447 0.961 pc/out\_3\_1 (pc/out\_3\_1)

LUT5:I0->O 18 0.203 1.049 ins\_mem/Mram\_instruction161 (ins<16>)

RAM32X1D:DPRA0->DPO 1 0.205 0.580 registers/Mram\_mem162 (registers/readRegister2[4]\_read\_port\_4\_OUT<31>)

LUT6:I5->O 3 0.205 0.755 registers/Mmux\_readData2251 (data2\_31\_OBUF)

LUT6:I4->O 1 0.203 0.000 alu/Mcompar\_in1[31]\_in2[31]\_equal\_2\_o\_lut<10> (alu/Mcompar\_in1[31]\_in2[31]\_equal\_2\_o\_lut<10>)

MUXCY:S->O 1 0.411 0.000 alu/Mcompar\_in1[31]\_in2[31]\_equal\_2\_o\_cy<10> (alu/in1[31]\_in2[31]\_equal\_2\_o)

FD:D 0.102 alu/zero

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Total 5.121ns (1.776ns logic, 3.345ns route)

(34.7% logic, 65.3% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 479 / 129

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Offset: 6.875ns (Levels of Logic = 4)

Source: pc/out\_3\_1 (FF)

Destination: data2<30> (PAD)

Source Clock: clk rising

Data Path: pc/out\_3\_1 to data2<30>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 2 0.447 0.961 pc/out\_3\_1 (pc/out\_3\_1)

LUT5:I0->O 18 0.203 1.049 ins\_mem/Mram\_instruction161 (ins<16>)

RAM32X1D:DPRA0->DPO 2 0.205 0.617 registers/Mram\_mem161 (registers/readRegister2[4]\_read\_port\_4\_OUT<30>)

LUT6:I5->O 2 0.205 0.616 registers/Mmux\_readData2241 (data2\_30\_OBUF)

OBUF:I->O 2.571 data2\_30\_OBUF (data2<30>)

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Total 6.875ns (3.631ns logic, 3.244ns route)

(52.8% logic, 47.2% route)

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Cross Clock Domains Report:

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Clock to Setup on destination clock clk

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

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clk | 5.121| | | |

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Total REAL time to Xst completion: 6.00 secs

Total CPU time to Xst completion: 6.27 secs

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Total memory usage is 4509832 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 120 ( 0 filtered)

Number of infos : 9 ( 0 filtered)